ABSTRACT OF THE DISCLOSURE

A clock signal can be synthesized by performing a clock and data recovery (CDR) operation on a potentially noisy clock source signal which has a known transition density. The CDR operation produces a desired clock signal in response to the clock source signal. In order to reduce crosstalk between plesiochronous receive and transmit clock domains of a serial data transceiver, a single common PLL is used both to recover the receive clock from the received data and to synthesize the transmit clock from a potentially noisy transmit clock source signal.